GAU 2813 $

PATENT
740756-1914

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Reexamination Application of:	)	Art Unit:	2813
Shunpei YAMAZAKI et al.	)	Examiner:	L. Schillinger
Application No.: 09/235,770	)		
Filed: January 25, 1999	)		
For: SEMICONDUCTOR DEVICE AND METHOD FOR FORMING THE SAME	)		

CERTIFICATE OF MAILING

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TRANSMITTAL LETTER

Commissioner of Patents
Washington, D.C. 20231

March 7, 2001

Dear Sir:

Transmitted herewith is an Amendment in the above-identified application.

The fees have been calculated as shown below:

	Claims Remaining After Amendment		Highest Number Previously Paid For	Present Extra	Small/Large Entity Rate	Fee
Total	36	Minus	36	0	x $9/$18	$0
Indep	8	Minus	8	0	x $40/$80	$0
First Presentation of Multiple Dependent Claim					+ $135/$270	$0
TOTAL						$0

B

[redacted]

[X] Also enclosed are Verified English Translations of Priority Documents JP 4-113027 and 4-124324; Petition for Extension of Time for three (3) Months; Information Disclosure Statement with PTO-1449 Form and References with English language Abstracts.

[X] A check in the amount of $970.00 is enclosed to cover Information Disclosure Statement fees and Extension of Time fees.

[X] In the event applicant(s) has overlooked the need for any petition and fee for extension of time, and such extension is required, applicant(s) requests that this be considered a petition therefor and that such fee be charged to Deposit Account No. 19-2380 (740756-1914).

[X] The Commissioner is hereby authorized to charge fees under 37 CFR 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c) and 1.20 (d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment, to Deposit Account No. 19-2380 (740756-1914). A duplicate copy of this sheet is attached.

Respectfully submitted,

NIXON PEABODY LLP

Reg. No. 38,434

Signed for:

Eric J. Robinson
Registration No. 38,285

8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
Phone (703) 770-9110
Fax (703) 883-0370

EJR/LCD:gjc
Attachments

B

[redacted]

Docket No. 0756-1914

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of)
Shunpei YAMAZAKI et al.)
Serial No.: 09/235,770) Group Art Unit: 2812
Filed: January 25, 1999) Examiner: S. Hawranek
For: SEMICONDUCTOR DEVICE AND)
METHOD FOR FORMING THE SAME)

VERIFICATION OF TRANSLATION

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

I, Ikuko Noda, 3-G, 1551, Hase, Atsugi-shi, Kanagawa-ken 243-0036 Japan, a translator, herewith declare:

that I am well acquainted with both the Japanese and English Languages;

that I am the translator of the attached translation of the Japanese Patent Application No. 4-113027 filed on April 6, 1992; and

that to the best of my knowledge and belief the following is a true and correct translation of the Japanese Patent Application No. 4-113027 filed on April 6, 1992.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: this 7th day of March, 2001

Ikuko Noda

Name: Ikuko Noda

[redacted]

[Name of Document]	Patent Application
[Reference Number]	P002085-01
[Filing Date]	April 6, 1992
[Attention]	Commissioner, Patent Office
[International Patent Classification]	G02F 1/00
[Title of Invention]	INSULATED GATE TYPE SEMICONDUCTOR DEVICE AND METHOD FOR FORMING THE SAME
[Number of Claims]	2

[Inventor]
[Address] 398, Hase, Atsugi-shi, Kanagawa-ken
c/o Semiconductor Energy Laboratory Co., Ltd.
[Name] Shunpei YAMAZAKI

[Inventor]
[Address] 398, Hase, Atsugi-shi, Kanagawa-ken
c/o Semiconductor Energy Laboratory Co., Ltd.
[Name] Hongyong ZHANG

[Applicant]
[Identification Number] 000153878
[Name] Semiconductor Energy Laboratory Co., Ltd.
[Representative] Shunpei YAMAZAKI

[List of Attachment]

[Attachment]	Specification	1
[Attachment]	Drawing	1
[Attachment]	Abstract	1

[redacted]

[NAME OF DOCUMENT] Specification
[TITLE OF THE INVENTION] INSULATED GATE TYPE SEMICONDUCTOR DEVICE AND METHOD FOR FORMING THE SAME
[WHAT IS CLAIMED IS]
[Claim 1] In an insulated gate field effect transistor having at least a semiconductor layer, an insulating film layer, and a gate electrode comprising a material selected from the group consisting of aluminum, chromium, titanium, tantalum, silicon, and an alloy thereof, which are provided on an insulating substrate, characterized in that the insulating film layer comprises a silicon oxide layer and a silicon nitride layer.

[Claim 2] A method for forming an insulated gate type semiconductor device comprising:
forming a semiconductor region on an insulating substrate;
forming a first insulating film mainly comprising silicon oxide on said semiconductor region;
forming a second insulating film mainly comprising silicon nitride on said first insulating film;
forming a metal film comprising a material selected from the group consisting of aluminum, chromium, titanium, tantalum, silicon, an alloy thereof on said second insulating film; and
forming an oxide layer on a surface of said metal film by making a current flow through said metal film in an electrolyte.

[DETAILED DESCRIPTION OF THE INVENTION]
[0001]
[FIELD FOR INDUSTRIAL USE]
The present invention relates to an insulated gate type semiconductor device, and particularly to a structure of a thin-film insulated gate type field effect transistor (TFT) and a method for producing the same.
[0002]
[DESCRIPTION OF THE PRIOR ART]
Recently, a thin-film insulated gate type field effect transistor (TFT) has been vigorously studied. For example, in Japanese Patent Application No. 4-30220 or No. 4-38637 invented by the present inventors, a TFT and a method of producing the same are disclosed. In the method, a gate electrode is formed of aluminum, titanium, chromium, tantalum or silicon. And the peripheral thereof is covered with aluminum oxide formed by the anodic oxidation method so that a source/drain is not overlapped with a gate electrode, that is, these elements are formed in an offset state, and the source/drain region is recrystallized by the laser annealing treatment.
[0003]
The TFT thus formed is proved to have a more excellent characteristic in comparison with a conventional silicon gate TFT having no offset or a TFT having a gate electrode which is formed of metal having a high melting point such as tantalum or chromium and is activated by a thermal

annealing. However, it is difficult to obtain this excellent characteristic with high reproducibility.
[0004]

One cause is due to the invasion of movable ions such as sodium from the external. The reproducibility is deteriorated by the invasion of sodium from the external, particularly in a process of forming a gate electrode of metal material such as aluminum or the like (using a sputtering or a electron beam deposition method), and in a subsequent anodic oxidation process. Particularly in the sputtering, there is contamination of sodium ions. However, the sputtering is superior in the mass production to the electron beam deposition method, and thus its use has been necessarily desirable to reduce a manufacturing cost.
[0005]

It has been known that sodium is blocked and gettered by phosphorus glass or the like. Therefore, a gate insulating film has been generally formed of phosphorus glass. However, it is difficult to form the phosphorus glass at a low temperature which is aimed by the inventions as disclosed in the above Patent Applications. In addition, if the formation of the phosphorus glass at such a low temperature is attempted, for example by injecting phosphorus into a silicon oxide gate insulating film using an ion doping method, there frequently occurs a problem that a large number of defects occur in the gate insulating film and thus the characteristic of the TFT is rather deteriorated.
[0006]

In addition, high voltage of 100 to 300V is required for the anodic oxidation, and thus there is a risk that the gate insulating film is damaged by the high voltage. That is, in the technical scope of the above mentioned patent applications, the gate insulating film is formed on a semiconductor film, and the gate electrode is formed on the gate insulating film. In this construction, a voltage occurs between the positively-charged gate electrode and the semiconductor film in a floating state in the anodic oxidation process. Therefore, as the resistance between the gate electrode and an electrolyte is increased in accordance with increase of the thickness of an anodic oxidation film on the gate electrode, the amount of current passing from the gate electrode through the gate insulating film and the semiconductor film to the electrolyte is increased. Accordingly, there occurs a case where the gate electrode is damaged by this current.
[0007]

[PROBLEMS TO BE SOLVED BY THE INVENTION]

The present invention intends to solve the problem. That is, an object of this invention is to prevent movable ions from invading from an external, and is to prevent the breakdown of a gate insulating film in order to improve the reliability.
[0008]

[MEANS TO SOLVE THE PROBLEM]

In the present invention, a silicon nitride film is interposed between an aluminum gate electrode and a gate insulating film. Assuming the composition ratio of silicon in the silicon nitride

film to 1, the composition ratio of nitrogen is in a range of 1 to 4/3, preferably in a range of 1.2 to 4/3. In addition to nitrogen and silicon, hydrogen or oxygen may be added.

[0009]

The silicon nitride film serves to block movable ions such as sodium, and thus can prevent the movable ions from invading from the gate electrode and other portions into a channel region. In addition, silicon nitride has higher conductivity than silicon oxide which is usually used for the gate insulating film, and thus the silicon nitride film also serves to prevent an excessive voltage from being applied between the gate electrode and the semiconductor region (channel region) beneath the gate electrode, so that breakdown of the gate insulating film can be prevented.

[0010]

Accordingly, the semiconductor region and the gate insulating film are formed, then the silicon nitride film is formed, and then an aluminum electrode is formed to form the gate electrode. The silicon nitride film is also preferable because when the silicon nitride film exists integrally over the entire surface of the substrate during the anodic oxidation of the aluminum electrode, the positive potential is kept to a substantially constant potential over the entire surface of the substrate.

The present invention will be described in more detail by illustrating examples as follows.

[0011]

[EMBODIMENT]

[EMBODIMENT 1]

Fig. 1 is cross-sectional views showing a manufacturing process of this embodiment. The detailed conditions of this embodiment are substantially the same as those of Japanese Patent Application No. 4-30220 or 4-38637 and thus the description thereof is eliminated. Firstly, an N-O glass produced by Nippon Electric Glass Co., Ltd. was used as a substrate 101. This glass has a high distortion temperature, but contains a large amount of lithium and sodium. Therefore, in order to prevent invasion of these movable ions from the substrate, a silicon nitride film 102 was formed in thickness of 10 to 50nm by a plasma CVD method or a low pressure CVD method. Further, a silicon oxide film 103 serving as a base film was formed in thickness of 100 to 800nm by a sputtering. An amorphous silicon film was formed thereon in thickness of 20 to 100nm by the plasma CVD method, and annealed at 600℃ for 12 to 72 hours at a nitrogen atmosphere to crystallize the amorphous silicon film. Subsequently, this result was subjected to a patterning process by the photolithography and the reactive ion etching (RIE) method, thereby forming island-like semiconductor regions 104 (for N-channel TFT) and 105 (for P-channel TFT) as shown in Fig. 1(A).

[0012]

Subsequently, a gate oxide film 106 was deposited in thickness of 50 to 200nm by a sputtering using silicon oxide as a target in an oxygen atmosphere, and then a silicon nitride film 107 was deposited in thickness of 2 to 20nm, preferably in thickness of 8 to 11nm by the plasma

CVD method or the low pressure CVD method.

[0013]

Thereafter, an aluminum film was formed by the sputtering or the electron beam deposition method, and then subjected to a patterning process with mixed acid (phosphoric acid solution added with 5% nitric acid) to form gate electrode/wirings 108 to 111. Through this process, an outline of the TFT was shaped.

[0014]

Further, a current was applied to the gate electrode/wirings 108 to 111 in the electrolyte to form aluminum oxide films 112 to 115 by the anodic oxidation method. An anodic oxidation condition as disclosed in Japanese Patent Application No. 4-30220 which was invented by the present inventors of this application, et al was adopted in this embodiment. Fig. 1(B) shows an intermediate produced in the above processes.

[0015]

Subsequently, an N-type impurity and a P-type impurity were injected into the semiconductor regions 104 and 105, respectively by a well-known ion injection method, thereby forming an N-type impurity region (source, drain) 116 and a P-type impurity region 117. This process was carried out using a well-known CMOS technique. A silicon nitride 107 at portions other than the portions beneath the gate electrode/wirings were removed by the reactive ion etching method. This process may be replaced by the wet etching treatment. In this case, by utilizing the difference in etching rate between aluminum oxide serving as the anodic oxide film and silicon nitride, the etching treatment is conducted in a self-aligned manner using aluminum oxide as a mask.

[0016]

Through these processes, the structure as shown in Fig. 1(D) was obtained. Naturally, the portion doped with the impurity by the ion injection method has low crystallinity, and thus it was substantially in a non-crystal state (amorphous state, or a polycrystal state close to the amorphous state). Therefore, a laser anneal treatment was conducted to improve crystallinity at the portion. This process may be carried out by a heat annealing treatment at 600 to 850℃. The same laser annealing condition as disclosed in Japanese Patent Application No. 4-30220 for example was adopted. After the laser annealing, the annealing treatment was conducted for 30 minutes to 3 hours at a temperature of 250 to 450℃ in a hydrogen atmosphere (1 to 700 torr, preferably 500 to 700 torr), thereby adding hydrogen to the semiconductor region to reduce lattice defects (dangling bond, etc.).

[0017]

In this way, the outline of the element was shaped. Afterwards, similarly in the ordinary manner, an interlayer insulator 118 was formed by the sputtering for silicon oxide film formation, and a hole for the electrode was formed by a well-known photolithography to expose the surface of the semiconductor region or the gate electrode/wiring. Finally, a second metal film (aluminum

or chromium) was selectively formed to form electrode/wirings 119 to 121. The first metal wirings 108 and 111 were crossed by the second metal wirings 119 and 121. Through the above mentioned process, NTFT 122 and PTFT 123 can be formed.

[0018]

[EMBODIMENT 2]

Fig. 2 is cross-sectional views showing a manufacturing process of this embodiment. The detailed conditions of this embodiment are substantially the same as those of Japanese Patent Application No. 4-30220 which was invented by the present inventors of this application, et al and thus the description thereof is eliminated. Firstly, an N-O glass produced by Nippon Electric Glass Co., Ltd. was used as a substrate 201 and a silicon nitride film 202 was formed in thickness of 10 to 50nm by a plasma CVD method or a low pressure CVD method. Further, a silicon oxide film 203 serving as a base film was formed in thickness of 100 to 800nm by a sputtering. An amorphous silicon film was formed thereon in thickness of 20 to 100nm by the plasma CVD method, and annealed at 600℃ for 12 to 72 hours in a nitrogen atmosphere to crystallize the amorphous silicon film. Subsequently, this result was subjected to a patterning process to form island-like semiconductor regions 204 (for N–channel TFT) and 205 (for P-channel TFT) as shown in Fig. 2(A).

[0019]

Subsequently, a gate oxide film 206 was deposited in thickness of 50 to 200nm by a sputtering, and then a silicon nitride film 207 was deposited in thickness of 2 to 20nm, preferably in thickness of 8 to 11nm by the plasma CVD method or the low pressure CVD method.

[0020]

Thereafter, an aluminum film was formed by a sputtering or an electron beam deposition method, and then subjected to a patterning process to form gate electrode/wirings 208 to 211. Through this process, an outline of the TFT was shaped as shown in Fig. 2(A).

[0021]

Further, a current was applied to the gate electrode/wirings 208 to 211 in the electrolyte to form aluminum oxide films 212 to 215 by the anodic oxidation method. The condition of the anodic oxidation as disclosed in Japanese Patent Application No. 3-30220 which was invented by the present inventors was adopted in this embodiment. Fig. 2(B) shows an intermediate produced in the above processes.

[0022]

Then, as shown in Fig. 2(C), silicon nitride 207 at portions other than the portions beneath the gate electrode/wirings and silicon oxide 206 were removed by the reactive ion etching method in order to expose semiconductor regions 204 and 205. This process may be replaced by the wet etching treatment. In this case, by utilizing the difference in etching rate among aluminum oxide serving as the anodic oxide film, silicon nitride, and silicon oxide, the etching treatment is conducted in a self-aligned manner using aluminum oxide as a mask. Further, by the laser doping

technique which was invented by the present inventors (Japanese Application No. 3-283981), an N-type impurity and a P-type impurity were injected into the semiconductor regions 204 and 205, respectively, thereby forming an N-type impurity region (source, drain) 216 and a P-type impurity region 217. This process was carried out using a CMOS technique disclosed in Japanese Patent Application No. 3-283981.

[0023]

Through these processes, the structure as shown in Fig. 2(D) was obtained. In a laser doping method, since an injection of impurity and annealing are conducted at the same time, there is no need to conduct the processes of laser annealing and heat annealing in the Embodiment 1. After the laser doping, the annealing treatment was conducted for 30 minutes to 3 hours at a temperature of 250 to 450℃ in a hydrogen atmosphere (1 to 700 torr, preferably 500 to 700 torr), thereby adding hydrogen to the semiconductor region to reduce lattice defects (dangling bond, etc.).

[0024]

In this way, the outline of the element was shaped. Afterwards, similarly in the ordinary manner, an interlayer insulator 218 was formed by the sputtering for silicon oxide formation, and a hole for the electrode was formed by a well-known photolithography to expose the surface of the semiconductor region or the gate electrode/wiring. Finally, a second metal film (aluminum or chromium) was selectively formed to form electrode/wirings 219 to 221. Through the above mentioned process, NTFT 222 and PTFT 223 can be formed.

[0025]

[EMBODIMENT 3]

Fig. 3 is cross-sectional views showing a manufacturing process of this embodiment. The detailed conditions of this embodiment are substantially the same as those of Japanese Patent Application No. 4-30220 and thus the description thereof is eliminated. Firstly, an N-O glass produced by Nippon Electric Glass Co., Ltd. was used as a substrate 301 and a silicon nitride film 302 was formed in thickness of 10 to 50nm by a plasma CVD method or a low pressure CVD method. Further, a silicon oxide film 303 serving as a base film was formed in thickness of 100 to 800nm by a sputtering. An amorphous silicon film was formed thereon in thickness of 20 to 100nm by the plasma CVD method, and annealed at 600℃ for 12 to 72 hours in a nitrogen atmosphere to crystallize the amorphous silicon film. Subsequently, this result was subjected to a patterning process to form island-like semiconductor regions 304 (for N–channel TFT) and 305 (for P-channel TFT) as shown in Fig. 3(A).

[0026]

Further, a gate oxide film 306 was deposited in thickness of 50 to 200nm by a sputtering, and then a silicon nitride film 307 was deposited in thickness of 2 to 20nm, preferably in thickness of 8 to 11nm by the plasma CVD method or the low pressure CVD method.

[0027]

Thereafter, an aluminum film was formed by a sputtering or an electron beam deposition method, and then subjected to a patterning process to form gate electrode/wirings 308 to 311. Through this process, an outline of the TFT was shaped as shown in Fig. 3(A).

[0028]

Further, a current was applied to the gate electrode/wirings 308 to 311 in the electrolyte to form aluminum oxide films 312 to 315 by the anodic oxidation method. An anodic oxidation condition as disclosed in Japanese Patent Application No. 4-30220 which was invented by the present inventors was adopted in this embodiment. Fig. 3(B) shows an intermediate produced in the above processes.

[0029]

Then, an N-type impurity and a P-type impurity were injected into the semiconductor regions 304 and 305, respectively by a well-known plasma ion doping method, thereby forming an N-type impurity region (source, drain) 316 and a P-type impurity region 317. This process was carried out using a well-known CMOS technique. In the plasma, hydrogen which was used as a dilute agent for gas source was ionized together with impurity elements, and injected into the semiconductor regions. This process may be carried out by a well-known ion injection method, however, this method requires a separate injection process of hydrogen ions for the reason as described later.

[0030]

Through these processes, the structure as shown in Fig. 3(D) was obtained. Naturally, the portion doped with the impurity by previous ion injection method has low crystallinity, and thus it is substantially in a non-crystal state (amorphous state, or a polycrystal state close to the amorphous state). Therefore, a laser anneal treatment was conducted to improve crystallinity at the portion. This process may be carried out by a heat annealing treatment at 600 to 850℃. The same condition of laser annealing condition as disclosed in Japanese Patent Application No. 4-30220 for example was adopted. However, XeCl laser (wavelength: 308nm) or XeF laser (wavelength: 351nm) is used because a silicon nitride film 307 does not transmit the ultraviolet rays having short wavelength of 250nm or less.

[0031]

After the laser annealing, the annealing treatment was conducted for 30 minutes to 3 hours at a temperature of 250 to 450℃ in a hydrogen atmosphere (1 to 700 torr, preferably 500 to 700 torr), thereby reducing lattice defects (dangling bond, etc.) in the semiconductor. Actually, delivery of hydrogen is little carried out between the inside of the semiconductor region and the outside thereof because the silicon nitride film 307 exists. Therefore, a large amount of hydrogen atoms are simultaneously injected into the semiconductor region in case of the plasma doping method, and on the other hand, in the case of the ion injection method, a process of injecting hydrogen atoms is separately required. If the amount of hydrogen atoms is insufficient, hydrogen atoms are required to be separately doped even in the plasma doping method.

[0032]

In this way, the outline of the element was shaped. Afterwards, similarly in the ordinary manner, an interlayer insulator 318 was formed by the sputtering for silicon oxide formation, and a hole for the electrode was formed by a well-known photolithography to expose the surface of the semiconductor region or the gate electrode/wiring. Finally, a second metal film (aluminum or chromium) was selectively formed to form electrode/wirings 319 to 321. Through the above mentioned process, NTFT 322 and PTFT 323 can be formed.

[0033]

[EMBODIMENT 4]

Fig. 2 shows an embodiment in which this invention was applied to a TFT having two-layered channel which was invented by the present inventors and described in applications filed on February 25, 1992 entitled "THIN FILM INSULATED GATE TYPE OF SEMICONDUCTOR DEVICE AND A PRODUCING METHOD THEREFOR" (applicant: Semiconductor Energy Laboratory Co., Ltd, three Patent Applications having docketing numbers : P002042-01 to P002044-03).

[0034]

That is, reference numerals 401, 501, and 601 show N-channel TFTs and 402, 402, and 402 show P-channel TFTs in Figs. 4, 5, and 6. In each figure, each first layers 408, 410, 508, 510, 508, and 510 was substantially formed of amorphous silicon in a thickness of 20 to 200nm.

[0035]

Reference numerals 407, 409, 507, 509, 607, and 609 represent silicon layers which were substantially in a polycrystal or semi-amorphous state, and the thickness of the silicon layers were set to 20 to 200nm. Further, reference numerals 404, 406, 504, 506, 604, and 606 represent gate insulating films formed of silicon oxide, and the thickness thereof was set to 50 to 300nm. Reference numerals 403, 405, 503, 505, 603, and 605 represent silicon nitride films each having 2 to 20nm thickness, which were formed in the same manner as the Embodiments 1 to 3. The construction of these elements were designed on the basis of the disclosure of the above Patent Application or the description of the Embodiment 1.

[0036]

[EFFECT OF THE INVENTION]

As mentioned above, by forming a silicon nitride film between gate electrode and gate insulating film, the present invention can prevent invasion of movable ions into a channel, and also prevent the breakdown of the gate insulating film while anodic oxidation of the gate electrode.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[Fig. 1] shows a process for producing a semiconductor device (cross section) according to the present invention.

[Fig. 2] shows a process for producing a semiconductor device (cross section) according to the present invention.

[Fig. 3] shows a process for producing a semiconductor device (cross section) according to the present invention.
[Fig. 4] shows an example of the structure of a semiconductor device according to the conventional example.
[Fig. 5] shows an example of the structure of a semiconductor device according to the conventional example.
[Fig. 6] shows an example of the structure of a semiconductor device according to the conventional example.

[EXPLANATION OF THE MARKS]

101	insulating substrate
102	blocking layer (silicon nitride)
103	blocking layer (silicon oxide)
104	semiconductor region (for N-channel TFT)
105	semiconductor region (for P-channel TFT)
106	gate insulating film
107	silicon nitride film
108 ~111	gate electrode/wirings (aluminum)
112~115	anodic oxide layers
116	N type impurity region
117	P type impurity region
118	interlayer insulator
119 ~121	second layer metal wirings
121	NTFT
122	PTFT

[NAME OF DOCUMENT] Abstract

[Abstract]

[Purpose]

It is an object of the present invention to form a stable thin film insulated gate type field effect having metal gate covered with an anodic oxide film, and to provide a method for preventing invasion of movable ions into a channel, in which thin film insulated gate type field effect transistor appropriate to the object is formed.

[Structure]

In a thin-film insulated gate type field effect transistor having a metal gate in which the surface of the gate electrode is subjected to anodic oxidation, a silicon nitride film is provided so as to be interposed between the gate electrode and the gate insulating film to prevent invasion of movable ions into a channel, and also to prevent the breakdown of the gate insulating film due to a potential difference between the gate electrode and the channel region.

[Selected figure] Fig. 1